What is claimed is:

1. A memory transistor comprising:
a substrate having a plurality of source/drain regions, the source/drain regions having a different conductivity type than the remainder of the substrate;
a metal floating gate overlying the substrate;
a metal oxide inter-gate insulator layer formed over the metal floating gate; the inter-gate insulator layer having a dielectric constant that is greater than a dielectric constant of silicon dioxide; and
a control gate formed on top of the inter-gate insulator layer.

2. The transistor of claim 1 and further including a high dielectric constant gate insulator layer between the substrate and the metal floating gate such that a composite gate insulator layer is formed by the gate insulator layer, the metal floating gate, and the inter-gate insulator layer.

3. The transistor of claim 2 wherein the composite gate insulator layer is comprised of deposited aluminum oxide – aluminum – aluminum oxide grown by oxidation.

4. The transistor of claim 3 wherein the aluminum oxide is grown by low temperature oxidation.

5. The transistor of claim 2 wherein the composite gate insulator layer is comprised of deposited aluminum oxide – aluminum – deposited aluminum oxide.

6. The transistor of claim 2 wherein the composite gate insulator layer is comprised of PbO – Pb – PbO wherein the PbO is grown by oxidation of Pb.

7. The transistor of claim 1 wherein the control gate is comprised of a metal.

8. A flash memory transistor comprising:

a substrate having a plurality of source/drain regions, the source/drain regions having a different conductivity than the remainder of the substrate;

a composite gate insulator layer, overlying the substrate, comprising a tunnel insulator, a metal floating gate and an inter-gate insulator formed from oxidation of metals, the tunnel insulator and the inter-gate insulator having a dielectric constant that is higher than silicon dioxide; and

a control gate formed on top of the inter-gate insulator.

9. The transistor of claim 8 wherein the inter-gate insulator is a metal oxide that is formed by one of: atomic layer deposition, chemical vapor deposition, or sputtering.

10. The transistor of claim 8 wherein the tunnel insulator comprises a perovskite oxide film.

11. The transistor of claim 8 wherein the inter-gate insulator is comprised of one of: Ta_2O_5, TiO_2, ZrO_2, or Nb_2O_5.

12. The transistor of claim 8 wherein the inter-gate insulator is formed by low temperature oxidation of a transition metal.

13. The transistor of claim 8 wherein the plurality of source/drain regions are comprised of an n+ type doped silicon.

14. The transistor of claim 8 wherein the control gate is a polysilicon material.

15. The transistor of claim 8 wherein the substrate is comprised of a p+ type silicon material.

16. The transistor of claim 8 wherein the composite gate insulator layer is comprised of one of the following structures: Ta_2O_5 –Ta – Ta_2O_5, TiO_2 – Ti – TiO_2, ZrO_2 – Zr – ZrO_2, or Nb_2O_5 – Zr – Nb_2O_5 wherein the metal oxide layers are formed by low temperature oxidation.

17. A flash memory transistor comprising:
a substrate having a plurality of source/drain regions, the source/drain regions having a different conductivity than the remainder of the substrate;
a high-k tunnel dielectric formed overlying the substrate;
a metal floating gate formed over the tunnel dielectric;
a high-k inter-gate insulator formed over the floating gate;
a control gate formed over the inter-gate insulator layer; and
a low dielectric constant oxide insulation area formed in the substrate on either side of each source/drain region.

18. The transistor of claim 17 wherein the substrate is comprised of a p+ type conductivity silicon and the source/drain regions are n+ doped regions in the substrate.

19. The transistor of claim 17 wherein the metal floating gate is comprised of Pb and the inter-gate insulator is PbO that is grown by oxidation of Pb.

20. A memory transistor array comprising:
a plurality of flash memory transistors organized in rows and columns, each row comprising:
a substrate having a plurality of source/drain regions organized in a column direction that is substantially perpendicular to the row, the source/drain regions having a different conductivity than the remainder of the substrate;
a high-k tunnel dielectric formed overlying the substrate;

a metal floating gate formed over the tunnel dielectric;

a high-k inter-gate insulator formed over the floating gate;

a control gate formed over the inter-gate insulator layer; and

a low dielectric constant oxide insulation area formed in the substrate on either side of each source/drain region; and

a low dielectric constant oxide isolation material separating the rows of the array.

21. An electronic system comprising:

a processor that generates control signals; and

a memory array coupled to the processor, the array comprising:

a plurality of flash memory transistors organized in rows and columns, each row comprising:

a substrate having a plurality of source/drain regions organized in a column direction that is substantially perpendicular to the row, the source/drain regions having a different conductivity than the remainder of the substrate;

a high-k tunnel dielectric formed overlying the substrate;

a metal floating gate formed over the tunnel dielectric;

a high-k inter-gate insulator formed over the floating gate;

a control gate formed over the inter-gate insulator layer; and

a low dielectric constant oxide insulation area formed in the substrate on either side of each source/drain region; and

a low dielectric constant oxide isolation material separating the rows of the array.

22. A method for fabricating a memory cell transistor, the method comprising:

creating a plurality of source/drain regions in a column direction by doping portions of a substrate;

creating a plurality of low dielectric constant oxide isolation areas in the substrate between each pair of source/drain regions;

forming a tunnel insulator over the substrate and between the oxide isolation areas, the tunnel insulator having a dielectric constant that is higher than silicon dioxide;

forming a metal floating gate over the tunnel insulator;

forming a metal oxide inter-gate insulator over the floating gate; and

forming a control gate over the inter-gate insulator.

23. The method of claim 22 wherein the plurality of source/drain regions are created with a p+ conductivity in an n+ substrate.

24. The method of claim 22 wherein the inter-gate insulator is comprised of a transition metal oxide that is formed by low temperature oxidation.

25. The method of claim 22 wherein the inter-gate insulator is comprised of one of Ta_2O_5, TiO_2, ZrO_2, or NbO_5.

26. The method of claim 22 wherein the inter-gate insulator is formed by one of atomic layer deposition, chemical vapor deposition, or sputtering.

27. The method of claim 22 wherein forming the inter-gate insulator comprises forming one of the following structures: $Ta_2O_5 - Ta - Ta_2O_5$, $TiO_2 - Ti - TiO_2$, $ZrO_2 - Zr - ZrO_2$, or $Nb_2O_5 - Zr - Nb_2O_5$ wherein the metal oxide layers are formed by low temperature oxidation.

28. The method of claim 22 wherein forming the inter-gate insulator comprises an evaporation technique prior to the low temperature metal oxidation.

29. The method of claim 22 wherein forming the gate insulator comprises an atomic layer deposition technique and an evaporation technique prior to the low temperature metal oxidation.